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Amendment and/or Response
Reply to Office action of 25 January 2006

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-20 (Canceled)

21. (New) A method comprising:

receiving a plurality of transform blocks in a sequential transform-block order,

converting each of the plurality of transform blocks into a plurality of bit-plane encodings,

storing each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks, and

transmitting each bit-plane encoding of the plurality of transform blocks in the sequential bit-plane order.

22. (New) The method of claim 21, wherein the sequential bit-plane order is from most-significant bit to least-significant bit of transform coefficients in each transform block.

23. (New) The method of claim 21, wherein the bit-plane encodings include a run-length encoding.

24. (New) The method of claim 21, wherein storing each bit-plane encoding in the memory includes storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored corresponding bit-plane encoding of a prior received transform block.

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25. (New) The method of claim 21, including

discarding each transform block after converting each of the bit-plane encodings for the transform block, and prior to transmitting a first bit-plane encoding of the plurality of transform blocks.

26. (New) The method of claim 21, wherein each transform block corresponds to a residual image of a fine granular scalability (FGS) encoding.

27. (New) The method of claim 21, wherein the transform blocks correspond to one of: a discrete cosine transform, a block-based wavelet transform, and a matching pursuit transform.

28. (New) The method of claim 21, wherein converting each transform block includes identifying a maximum transform coefficient within the transform block, and determining the plurality of bit-plane encodings for the transform block based on the maximum transform coefficient.

29. (New) An apparatus comprising:

a memory,

a converter that is configured to:

receive a plurality of transform blocks in a sequential transform-block order,

convert each of the plurality of transform blocks into a plurality of bit-plane encodings, and

store each of the plurality of bit-plane encodings in a sequential bit-plane order of the memory prior to converting another of the plurality of transform blocks.

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30. (New) The apparatus of claim 29, including

a transmitter that is configured to transmit each bit-plane encoding of the plurality of transform blocks in the sequential bit-plane order.

31. (New) The apparatus of claim 29, wherein the sequential bit-plane order is from most-significant bit to least-significant bit of transform coefficients in each transform block.

32. (New) The apparatus of claim 29, wherein the bit-plane encodings include a run-length encoding.

33. (New) The apparatus of claim 29, wherein the converter is configured to:

store a first bit-plane encoding of a first transform block at a first location of the memory and a second bit-plane encoding of the first transform block at a second location of the memory, and

store a corresponding first bit-plane encoding of a second transform block at a third location that is between the first and second locations of the memory.

34. (New) The apparatus of claim 33, wherein the third location is immediately adjacent the first location.

35. (New) The apparatus of claim 29, wherein each transform block corresponds to a residual image of a fine granular scalability (FGS) encoding.

36. (New) The apparatus of claim 29, wherein the transform blocks correspond to one of: a discrete cosine transform, a block-based wavelet transform, and a matching pursuit transform.

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37. (New) The apparatus of claim 29, wherein the converter is configured to:

determine a maximum transform coefficient within the transform block, and

determine the plurality of bit-plane encodings for the transform block based on the maximum transform coefficient.

38. (New) A computer readable medium that includes computer program code, which, when executed on a processor, enables the processor to:

receive a plurality of transform blocks in a sequential transform-block order,

convert each of the plurality of transform blocks into a plurality of bit-plane encodings, and

store each of the plurality of bit-plane encodings in a sequential bit-plane order of a memory prior to converting another of the plurality of transform blocks.

39. (New) The computer readable medium of claim 38, wherein the processor is enabled to:

store a first bit-plane encoding of a first transform block at a first location of the memory and a second bit-plane encoding of the first transform block at a second location of the memory, and

store a corresponding first bit-plane encoding of a second transform block at a third location that is between the first and second locations of the memory.

40. (New) The computer readable medium of claim 38, wherein the bit-plane encodings include a run-length encoding.